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Sir:

Transmitted herewith for filing under 37 C.F.R. § 1.53(b) is the nonprovisional utility patent application of:

Motoyasu TAGUCHI

Enclosed are:

[X] Specification, Claim(s), and Abstract (22 pages).

[X] Formal drawings (9 sheets, Figures 1-8).

[X] Declaration and Power of Attorney (2 pages).

[X] Assignment of the invention to NEC CORPORATION.

[X] Assignment Recordation Cover Sheet.

[X] Claim for Convention Priority and Priority Document.

The filing fee is calculated below:

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Basic Fee							$690.00		$690.00
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Independents:	6	-	3	=	3	x	$78.00	=	$234.00
If any Multiple Dependent Claim(s) present:						+	$260.00	=	$0.00
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Respectfully submitted,

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RECEIVING TERMINAL, RECEIVER AND RECEIVING METHOD FOR CDMA SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to receiving terminals, receivers and receiving methods for CDMA (Code Division Multiple access) system and, more particularly, receiving terminals for CDMA system capable of reducing the power consumption.

Fig. 8 is a block diagram showing a prior art receiving terminal for CDMA system. The receiving terminal for CDMA system comprises an antenna 110, a radio circuit 120, a finger circuit 130 including a plurality of (i.e., six in the illustrated example) finger circuit elements, a lake circuit 140 including a synthesizer and a level measuring circuit, a timing circuit 150, a Viterbi circuit 160, a codec circuit 170, a loudspeaker 180 and a crystal oscillator 190.

The finger circuit 130 includes six finger circuit elements (1) to (6), which each obtain a correlation between a received signal fed out from the radio circuit 120 and a known signal and feed out the resultant correlated value of the received signal to the lake circuit 140. The timing circuit 150 determines the timings for obtaining the correlated values in the finger circuit 130. The individual finger circuit elements (1) to (6) obtain the correlated values under control of a pulse signal fed out for every 10 msec. from the timing circuit 150 as trigger. The lake circuit 140 executes

synthesis of the correlated values of the received signal and level measurement. The Viterbi circuit 160 executes error correction of the synthesized received signal from the lake circuit 140. The codec circuit 170 converts the corrected received signal from the lake circuit 140 to a voice signal, which is fed out to the loudspeaker 180 for outputting voice. The crystal oscillator 190 generates clocks for controlling the operation of various components.

In the prior art described above, however, the finger circuit 130 and timing circuit 150 operate independently of level of the received signal. This leads to a problem that the power consumption is increased or high.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a receiving terminal, a receiver and receiving method for CDMA system capable of reducing the power consumption.

According to an aspect of the present invention, there is provided a receiving terminal for CDMA system comprising at least a finger circuit for taking a correlation of a received signal from a radio circuit connected to an antenna and known signal and feeding out the correlated received signal, and a lake circuit for combining a plurality of outputs from the finger circuits and executing level measurement, wherein: the lake circuit includes a level judgment circuit for executing

electric field judgment according to the correlated received signal from the finger circuit and a predetermined threshold level, the operation of a predetermined circuit being suspended according to the result of the level judgment.

The operation control clock supply to the finger circuit is suspended for power consumption reduction according to the result of the level judgment in the level judging circuit. The operation control clock supply to a timing circuit in the finger circuit is suspended according to the result of level judgment in the level judging circuit. The operation control clock supply is suspended after the lapse of a predetermined period of time. The operation control clock supply to the finger circuit or to the timing circuit therein is resumed after the lapse of predetermined period of time.

The threshold value is preset in a memory. The memory is an E^2PROM, and threshold data therefrom is supplied under CPU control to the lake circuit. The finger circuit takes correlation of output signal data fed out from the radio circuit and known signal data to each other, demodulates the correlated data to symbol unit data, and feeds out the demodulated data to the lake circuit. The level measurement is executed by computing the power level in a pilot symbol part in one frame for each slot and adding together the results of the computation for one frame. The finger circuit includes a plurality of finger circuit elements, which each

obtains the difference of the maximum level and a pertinent level among the electric field levels in them and compare the difference and the threshold value with each other.

According to another aspect of the present invention, there is provided a receiving terminal for CDMA system for receiving received signals from a plurality of signal propagation channels, wherein: the electric field level of the received signal from each signal propagation channel is judged, and the operation control clock supply to a circuit system receiving signal from a low electric field level signal propagation channel is suspended for a predetermined period of time for power consumption reduction.

According to other aspect of the present invention, there is provided a receiver for CDMA system comprising at least a finger circuit for taking a correlation of a received signal from a radio circuit connected to an antenna and known signal and feeding out the correlated received signal, and a lake circuit for combining a plurality of outputs from the finger circuits and executing level measurement, wherein:

the lake circuit includes a level judgment circuit for executing electric field judgment according to the correlated received signal from the finger circuit and a predetermined threshold level, the operation of a predetermined circuit being suspended according to the result of the level judgment.

Various modifications may be employed in accordance with the above ways.

According to still other aspect of the present invention, there is provided a receiver for CDMA system for receiving received signals from a plurality of signal propagation channels, wherein:

the electric field level of the received signal from each signal propagation channel is judged, and the operation control clock supply to a circuit system receiving signal from a low electric field level signal propagation channel is suspended for a predetermined period of time.

According to further aspect of the present invention, there is provided a receiving method for CDMA system with step for taking a correlation of a received signal and known signal and combining a plurality of correlated signals for level measurement, the method further comprising:

executing electric field judgment according to the correlated received signal and a predetermined threshold level, and suspending an operation of a predetermined circuit according to the result of the level judgment.

According to still further aspect of the present invention, there is provided a receiving method for CDMA system for receiving received signals from a plurality of signal propagation channels including steps of:

judging the electric field level of the received signal from each signal propagation channel; and

suspending the operation control clock supply to a circuit receiving signal from a low electric field level signal propagation channel for a predetermined period of time.

Other objects and features will be clarified from the following description with reference to attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a preferred embodiment of the receiving terminal for CDMA system according to the present invention;

Fig. 2 is a block diagram showing details of the lake circuit 40 shown in Fig. 1;

Fig. 3 is a schematic illustrating a correlating process in the finger circuit 30 shown in Fig. 1; and

Fig. 4 illustrates the operation of the finger circuit 30;

Figs. 5A and 5B are flow charts showing the operation of CDMA receiving terminal according to the present invention;

Fig. 6 shows the configuration of pilot symbol part and data part in one frame;

Fig. 7 shows the pass selection example of CDMA receiving terminal in Fig. 1; and

Fig. 8 is a block diagram showing a prior art receiving terminal for CDMA system.

PREFERRED EMBODIMENTS OF THE INVENTION

Preferred embodiments of the present invention

will now be described with reference to the drawings.

In the receiving terminal for CDMA system according to the present invention, when receiving signals from a plurality of signal propagation channels, the lake circuit, particularly a level judging circuit therein, judges the electric field level of the received signal from each signal propagation channel. Using the results of the level judgment, the supply of the operation clock to the circuit, which receives the signal from the propagation channel with lower electric level, is stopped at a constant time, thus reducing the power consumption.

As shown in Fig. 1, the receiving terminal for CDMA system comprises a CPU 52 and a memory (E^2PROM) 54 in addition to an antenna 10, a radio circuit 20, a finger circuit 30 having a plurality of finger circuit elements (1) to (6), a lake circuit 40, a timing circuit 50, a Viterbi circuit 60, a codec circuit 70, a loudspeaker 80 and a crystal oscillator 90.

As shown in Fig. 2, the lake circuit 40 has a main synthesizer 41, a sub-synthesizer 42, a level measuring circuit 43, a path level judging circuit 44, a level judging circuit 45 and a path selecting circuit 46. Each finger circuit element in the finger circuit 30 has a multiplifier 31 for multiplifying the received signal and known data by each other, a buffer (or memory) 33 and an adder for adding together the outputs of the multiplifier 31 and the buffer 33.

The finger circuit elements (1) to (6) in the finger circuit 30 are each connected to the lake circuit 40, the radio circuit 20 and the timing circuit 50. Each element receives the received signal from the radio circuit 20 under control of a timing pulse signal from the timing circuit 50 as trigger. Each element then correlates the received signal input with the known data, and informs the result of the correlation to the lake circuit 40. The timing circuit 50 is connected to the finger circuit 30, and feeds out a timing pulse signal to each of the elements (1) to (6) in the finger circuit 30 for every 10 msec. The CPU 52 is connected to the lake circuit 40, and feeds out threshold data read out from the memory (i.e., E^2PROM) 54 to the lake circuit 40.

The Viterbi circuit 60 executes error correction of the synthesized received signal from the lake circuit 40. The codec circuit 70 convert the corrected received signal from the Viterbi circuit 60 to a voice signal, which is fed out to the loudspeaker 80 for outputting voice. The crystal oscillator 90 supplies an operation control clock to each component of the circuit. The memory (or E^2PROM) 54 is a programmable read-only memory for preserving (or storing) threshold data set in the lake circuit 40 and capable of electrically erasing the stored data.

The lake circuit 40 shown in Fig. 2 will now be described. The main synthesizer 41 combines the results of correlation fed out from the finger circuit 30. The

level measuring circuit 43 computes electric field levels from the correlation results from the finger circuit 30. When an electric field level computed in the level measuring circuit 43 exceeds a threshold level, the path level judging circuit 44 instructs the path selecting circuit 46 not to feed out the received signal from the pertinent finger circuit element to the sub-synthesizer 42. The path selecting circuit 46 feeds out the received signal from each of the elements (1) to (6) in the finger circuit 30 to the sub-synthesizer 42 according to a control signal designated by the path level judging circuit 46.

The sub-synthesizer 42 executes synthesis of each path fed out from the path selecting circuit 46, and feeds out the result to the level judging circuit 45. The level judging circuit 45 compares the outputs from the main synthesizer 41 and the sub-synthesizer 42. Thus, when a difference in excess of a certain fixed value is present, the circuit 45 generates a control signal for discontinuing the operation control clock supply to the finger circuit 30.

Usually, when receiving signals from a plurality of signal propagation paths, the finger circuit 30 is operated according to the number of signal propagation paths and the received signal level in each signal propagation path. At this time, the finger circuit 30 takes correlation between each signal fed out from the radio circuit 20 and known signal, and feeds out the

correlated value of the received signal to the lake circuit 40. The lake circuit 40 combines the correlated values of the received signal fed out from the elements (1) to (6) of the finger circuit 30 to obtain a synthesized signal, which is fed out to the Viterbi circuit 60 for error correction and then fed out to the codec circuit 70 for conversion to voice signal for the voice output from the loudspeaker 80. The lake circuit 40 measures the levels of the correlated received signals from the elements (1) to (6) in the finger circuit 30, and feeds out a control signal to other circuits according to the results of measurements.

In the receiving terminal for CDMA system according to the present invention, the lake circuit 40 includes the level judging circuit 45. The level judging circuit 45 compares the levels of the correlated received signal fed out from each of the elements (1) to (6) of the finger circuit 30 and a threshold value. When the correlated received signal level is higher than the threshold value, the circuit 45 generates a control signal for suspending the clock supply to the pertinent element in the finger circuit 30 for a predetermined period of time. After the lapse of the predetermined period of time, the element in the finger circuit 30 which has suspended the clock supply, is restored to provide the level judging function again.

The finger circuit 30 takes correlation between each output signal from the radio circuit 20 and known

signal, and feeds out the correlated value of the received signal (step S1 in Fig. 5). Fig. 4 illustrates the operation of the finger circuit 30. The finger circuit 30 receives each received signal under control of pulse signal fed out from the timing circuit 50 for every 10 msec. (T0 in Fig. 4). At this time, the circuit 30 takes correlation of known data and received data to each other (T1 in Fig. 45), then demodulates the resultant correlated data to symbol unit data, and feeds out this data to the lake circuit 40 (T2 in Fig. 4). Further, as schematically shown in Fig. 3, the mulitiplier 31 in the finger circuit 30 multiplies the known data and received data by each other in units of 61 nsec. The symbol adder 32 addes together the product data from the circuit 30 and data of the buffer 33. This process of addition is executed in one symbol unit to compute the power levels of I and Q signals.

The level measuring circuit 43 executes the level measurement by using normally transmitted data part (pilot symbol). Fig. 6 shows the configuration of pilot symbol part and data part in one frame (10 msec.). The pilot symbol part is a power (level) computing subject. Each pilot symbol part and data symbol part constitute a slot unit of 0.625 msec. The level measuring circuit 43 computes the power level of the pilot symbol part for each of the elements (1) and (6) of the finger circuit 30 for every slot. The circuit 43 adds together the result of computation for one frame, and feeds out the

sum result to the path level judging circuit 44 (step S2 in Fig. 5).

The path level judging circuit 44 obtains the difference between the maximum level and each of the other levels as the electric field levels in the elements (1) to (6) of the finger circuit 30, and compares the difference with threshold value Tp (step S3 in Fig. 5). Fig. 7 shows the way of comparison. When the difference is above the threshold, the path level judging circuit 44 controls the path selecting circuit 46 such that no received signal is fed out from the pertinent finger circuit to the sub-synthesizer 42 (step S4 in Fig. 5). In other words, the sub-synthesizer 42 combines only path higher by a constant value than the other levels, and feeds out the resultant synthesized data to the level judging circuit 45 (step S5 in Fig. 5A).

Fig. 7 shows an example of the results of path level measurement in the path level measuring circuit 43 while the operation control clock is supplied to each element (1) to (6) of the finger circuit 30. In the Figure, the ordinate is taken for signal level, the abscissa is taken for time. In the example as shown, only paths 3 and 6 are within the threshold value Tp with respect to the maximum level path 4. Thus, in this case, these paths 3, 4 and 6 are subjects of synthesis in the sub-synthesizer 42.

The main synthesizer 41 combines the levels of all the received signals in the elements (1) to (6) of the

finger circuit 30. The level judging circuit 45 computes the difference between the result outputs of the main synthesizer 41 and sub-synthesizer 42 (step S7 in Fig. 5). The level judging circuit 45 judges whether the computed difference is within the threshold value Tg (step S8 in Fig. 5). If this difference is within the threshold value Tg (Yes), the path level judging circuit 45 decides that suspending the operation control clock supply to the finger circuit corresponding to the path selected by the path level judging circuit 44 has no adverse effects on the reception quality, and generates a control signal for suspending the operation control clock supply to the pertinent element of the finger circuits (step S9 in Fig. 5).

The level judging circuit 45 also retrieves for an element, if any, of the finger circuit 30, to which the operation control clock supply is suspended (step S10 in Fig. 5). If any element without operation control clock supply thereto is present, the circuit 45 checks whether a predetermined period of time (10×n ms) has passed after the suspension of the operation control clock supply to that element (step S11 in Fig. 5). When the predetermined period of time has passed since the suspension (Yes), the circuit 45 resumes or restores the operation control clock supply to the pertinent element of the finger circuit (step S12 in Fig. 5). When "No" yields in the steps S10 and S11 and also after the step S12, the routine returns to the step S1.

Then, the main synthesizer 41 combines the correlated received signals from the elements (1) to (6) in the finger circuit 30, and feeds out the synthesized signal to the Viterbi circuit 60. The Viterbi circuit 60 executes error correction of the synthesized received signal, and feeds out the corrected received signal to the codec circuit 79. The codec circuit 70 converts the received signal to voice signal for voice output from the loudspeaker 80.

In the embodiment shown in Fig. 1, the elements (1) and (6) in the finger circuit 30 operates under control of a timing control signal from the timing circuit 50 as trigger. Thus, when the result of correlation informed from the elements (1) to (6) of the finger circuit 30 is above the threshold, it is not only possible to suspend the operation control clock supply to the pertinent element of the circuit 30 for a predetermined period of time.

As has been understood from the foregoing description, with the receiving terminal for CDMA system according to the present invention it is possible to obtain the following pronounced effects in practice.

First, it is possible reduce power consumption compared to the prior art receiving terminal for CDMA system. This is so because in the case when the correlated value of the received signal fed out from each element of the finger circuit is above the threshold the operation control clock supply to that element is

suspended.

Secondly, the receiving terminal for CDMA system is obtainable by merely adding the level judging circuit for suspending the operation control clock supply to the lake circuit used in the prior art receiving terminal for CDMA system. The construction is thus simple and is inexpensively realizable.

Changes in construction will occur to those skilled in the art and various apparently different modifications and embodiments may be made without departing from the scope of the present invention. The matter set forth in the foregoing description and accompanying drawings is offered by way of illustration only. It is therefore intended that the foregoing description be regarded as illustrative rather than limiting.

What is claimed is:

1. A receiving terminal for CDMA system comprising at least a finger circuit for taking a correlation of a received signal from a radio circuit connected to an antenna and known signal and feeding out the correlated received signal, and a lake circuit for combining a plurality of outputs from the finger circuits and executing level measurement, wherein:

the lake circuit includes a level judgment circuit for executing electric field judgment according to the correlated received signal from the finger circuit and a predetermined threshold level, the operation of a predetermined circuit being suspended according to the result of the level judgment.

2. The receiving terminal for CDMA system according to claim 1, wherein the operation control clock supply to the finger circuit is suspended for power consumption reduction according to the result of the level judgment in the level judging circuit.

3. The receiving terminal for CDMA system according to claim 1, wherein the operation control clock supply to a timing circuit in the finger circuit is suspended according to the result of level judgment in the level judging circuit.

4. The receiving terminal for CDMA system according

to claim 1, wherein the operation control clock supply is suspended after the lapse of a predetermined period of time.

5. The receiving terminal for CDMA system according to claim 1, wherein the operation control clock supply to the finger circuit or to the timing circuit therein is resumed after the lapse of predetermined period of time.

6. The receiving terminal for CDMA system according to claim 1, wherein the threshold value is preset in a memory.

7. The receiving terminal for CDMA system according to 4, wherein the memory is an E2PROM, and threshold data therefrom is supplied under CPU control to the lake circuit.

8. The receiving terminal for CDMA system according to claim 1, wherein the finger circuit takes correlation of output signal data fed out from the radio circuit and known signal data to each other, demodulates the correlated data to symbol unit data, and feeds out the demodulated data to the lake circuit.

9. The receiving terminal for CDMA system according to claim 1, wherein the level measurement is executed by computing the power level in a pilot symbol part in one

frame for each slot and adding together the results of the computation for one frame.

10. The receiving terminal for CDMA system according to claim 1, wherein the finger circuit includes a plurality of finger circuit elements, which each obtains the difference of the maximum level and a pertinent level among the electric field levels in them and compare the difference and the threshold value with each other.

11. A receiving terminal for CDMA system for receiving received signals from a plurality of signal propagation channels, wherein:

the electric field level of the received signal from each signal propagation channel is judged, and the operation control clock supply to a circuit system receiving signal from a low electric field level signal propagation channel is suspended for a predetermined period of time for power consumption reduction.

12. A receiver for CDMA system comprising at least a finger circuit for taking a correlation of a received signal from a radio circuit connected to an antenna and known signal and feeding out the correlated received signal, and a lake circuit for combining a plurality of outputs from the finger circuits and executing level measurement, wherein:

the lake circuit includes a level judgment circuit

for executing electric field judgment according to the correlated received signal from the finger circuit and a predetermined threshold level, the operation of a predetermined circuit being suspended according to the result of the level judgment.

13. The receiver for CDMA system according to claim 12, wherein the operation control clock supply to the finger circuit is suspended for power consumption reduction according to the result of the level judgment in the level judging circuit.

14. The receiver for CDMA system according to claim 12, wherein the operation control clock supply to a timing circuit in the finger circuit is suspended according to the result of level judgment in the level judging circuit.

15. The receiver for CDMA system according to claim 12, wherein the operation control clock supply is suspended after the lapse of a predetermined period of time.

16. The receiver for CDMA system according to claim 12, wherein the operation control clock supply to the finger circuit or to the timing circuit therein is resumed after the lapse of predetermined period of time.

17. The receiver for CDMA system according to claim

12, wherein the threshold value is preset in a memory.

18. The receiver for CDMA system according to 15, wherein the memory is an E2PROM, and threshold data therefrom is supplied under CPU control to the lake circuit.

19. The receiver for CDMA system according to claim 12, wherein the finger circuit takes correlation of output signal data fed out from the radio circuit and known signal data to each other, demodulates the correlated data to symbol unit data, and feeds out the demodulated data to the lake circuit.

20. The receiver for CDMA system according to claim 12, wherein the level measurement is executed by computing the power level in a pilot symbol part in one frame for each slot and adding together the results of the computation for one frame.

21. The receiver for CDMA system according to claim 12, wherein the finger circuit includes a plurality of finger circuit elements, which each obtains the difference of the maximum level and a pertinent level among the electric field levels in them and compare the difference and the threshold value with each other.

22. A receiver for CDMA system for receiving

received signals from a plurality of signal propagation channels, wherein:

the electric field level of the received signal from each signal propagation channel is judged, and the operation control clock supply to a circuit system receiving signal from a low electric field level signal propagation channel is suspended for a predetermined period of time.

23. A receiving method for CDMA system with step for taking a correlation of a received signal and known signal and combining a plurality of correlated signals for level measurement, the method further comprising:

executing electric field judgment according to the correlated received signal and a predetermined threshold level, and suspending an operation of a predetermined circuit according to the result of the level judgment.

24. A receiving method for CDMA system for receiving received signals from a plurality of signal propagation channels including steps of:

judging the electric field level of the received signal from each signal propagation channel; and

suspending the operation control clock supply to a circuit receiving signal from a low electric field level signal propagation channel for a predetermined period of time.

ABSTRACT OF THE DISCLOSURE

A receiving terminal for CDMA system for receiving received signals from a plurality of signal propagation channels is disclosed. The electric field level of the received signal from each signal propagation channel is judged, and the operation control clock supply to a circuit system receiving signal from a low electric field level signal propagation channel is suspended for a predetermined period of time for power consumption reduction.

FIG.1

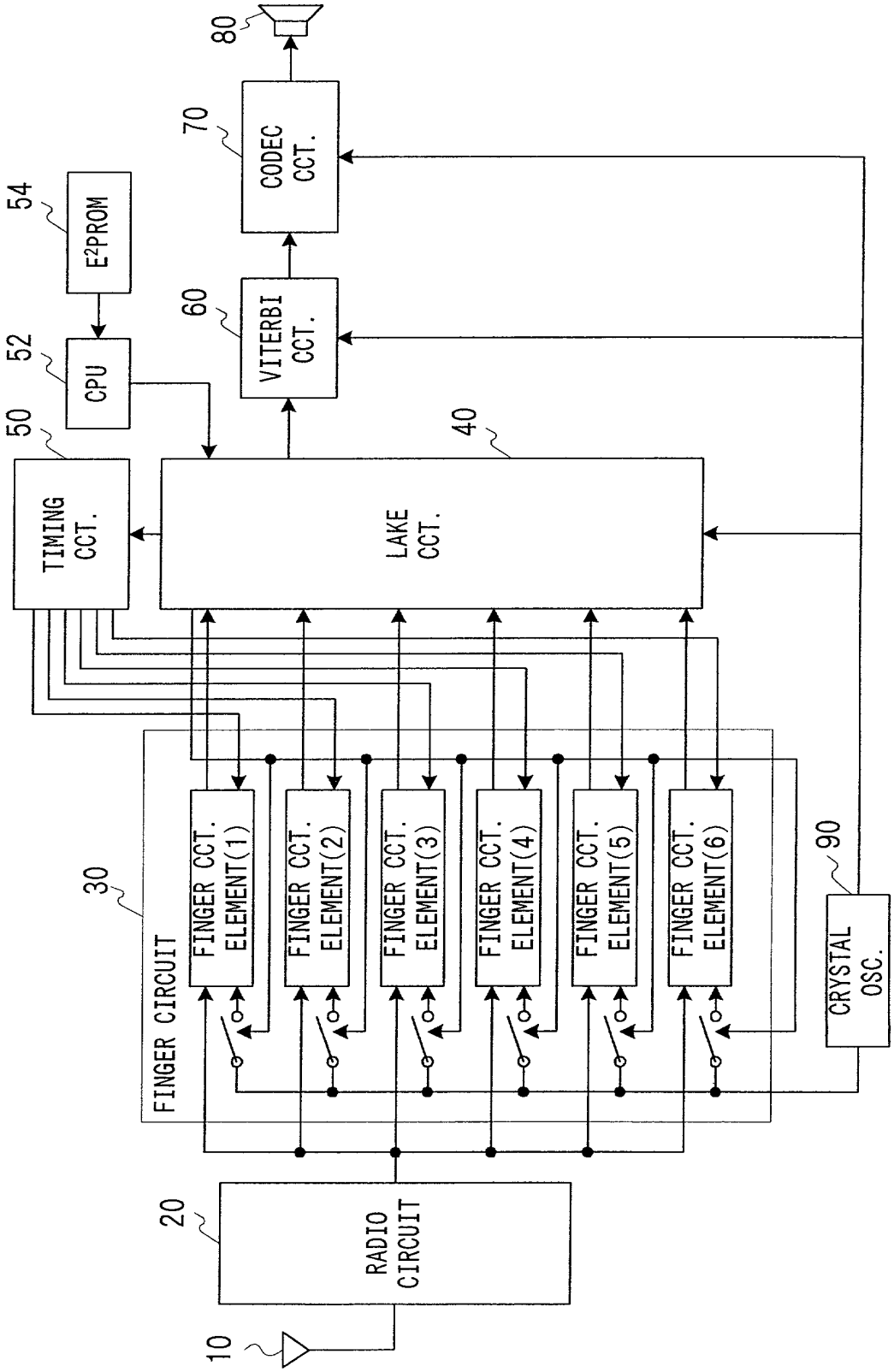

10
20
RADIO CIRCUIT
30
FINGER CIRCUIT
FINGER CCT. ELEMENT(1)
FINGER CCT. ELEMENT(2)
FINGER CCT. ELEMENT(3)
FINGER CCT. ELEMENT(4)
FINGER CCT. ELEMENT(5)
FINGER CCT. ELEMENT(6)
40
LAKE CCT.
50
TIMING CCT.
52
CPU
54
E²PROM
60
VITERBI CCT.
70
CODEC CCT.
80
90
CRYSTAL OSC.

FIG.2

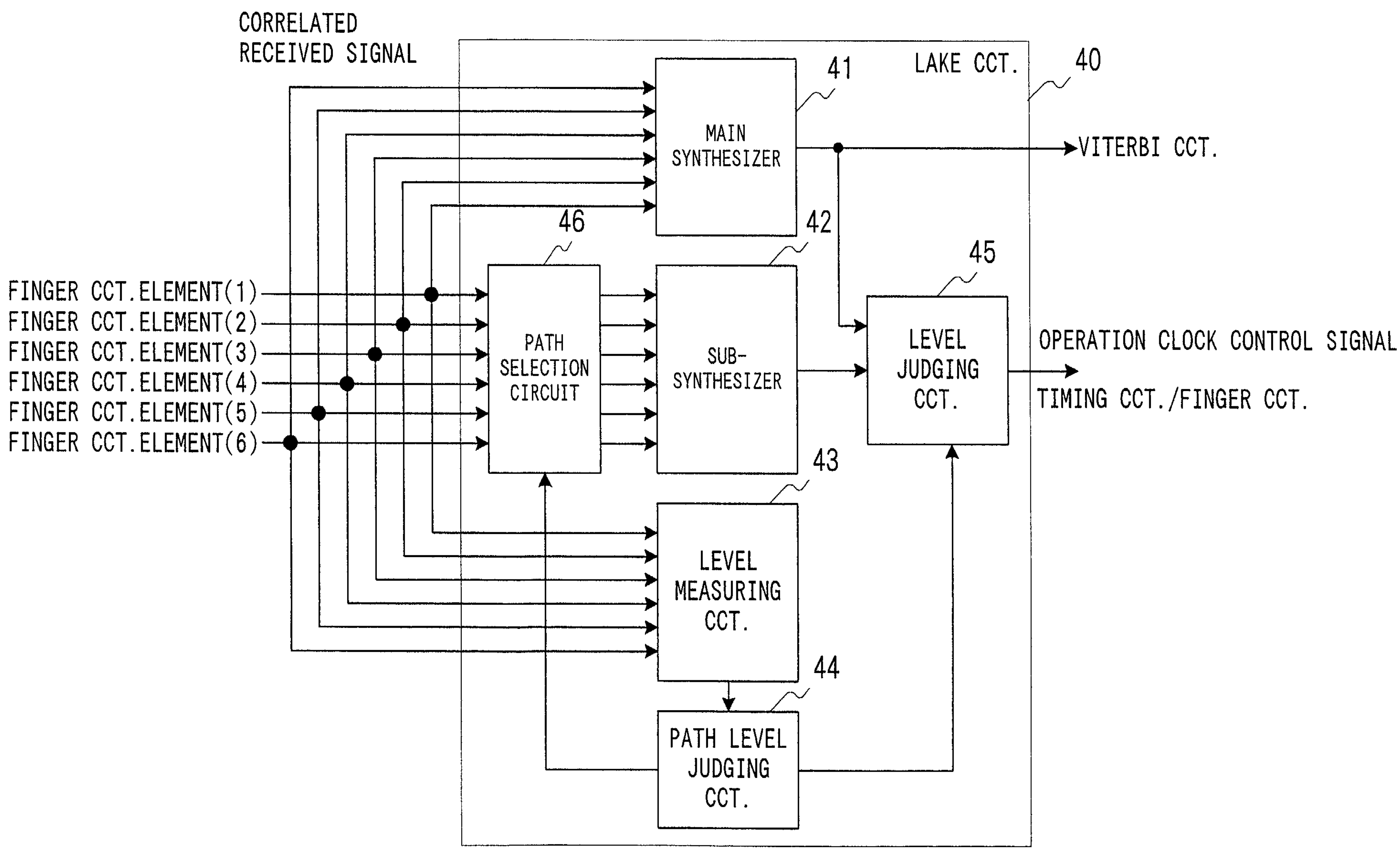

CORRELATED
RECEIVED SIGNAL
LAKE CCT.
40
41
MAIN
SYNTHESIZER
VITERBI CCT.
46
42
45
FINGER CCT.ELEMENT(1)
FINGER CCT.ELEMENT(2)
FINGER CCT.ELEMENT(3)
FINGER CCT.ELEMENT(4)
FINGER CCT.ELEMENT(5)
FINGER CCT.ELEMENT(6)
PATH
SELECTION
CIRCUIT
SUB-
SYNTHESIZER
LEVEL
JUDGING
CCT.
OPERATION CLOCK CONTROL SIGNAL
TIMING CCT./FINGER CCT.
43
LEVEL
MEASURING
CCT.
44
PATH LEVEL
JUDGING
CCT.

FIG.3

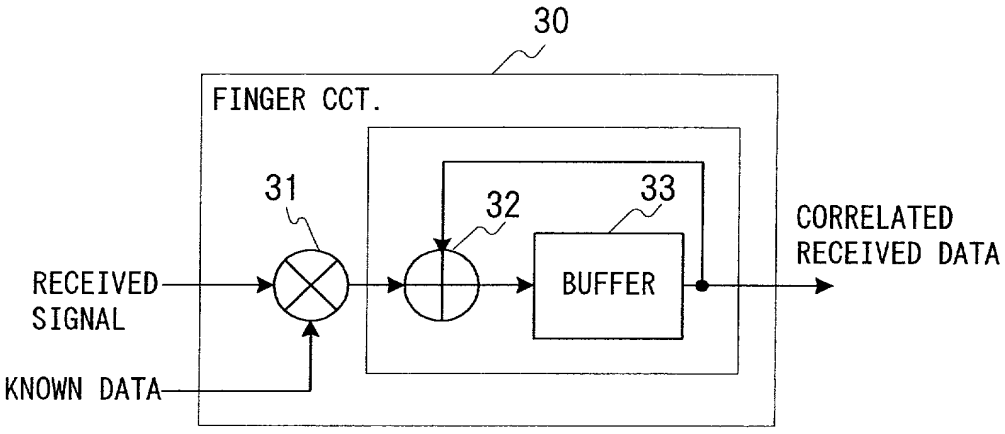

30
FINGER CCT.
31
32
33
BUFFER
RECEIVED
SIGNAL
KNOWN DATA
CORRELATED
RECEIVED DATA

FIG.4

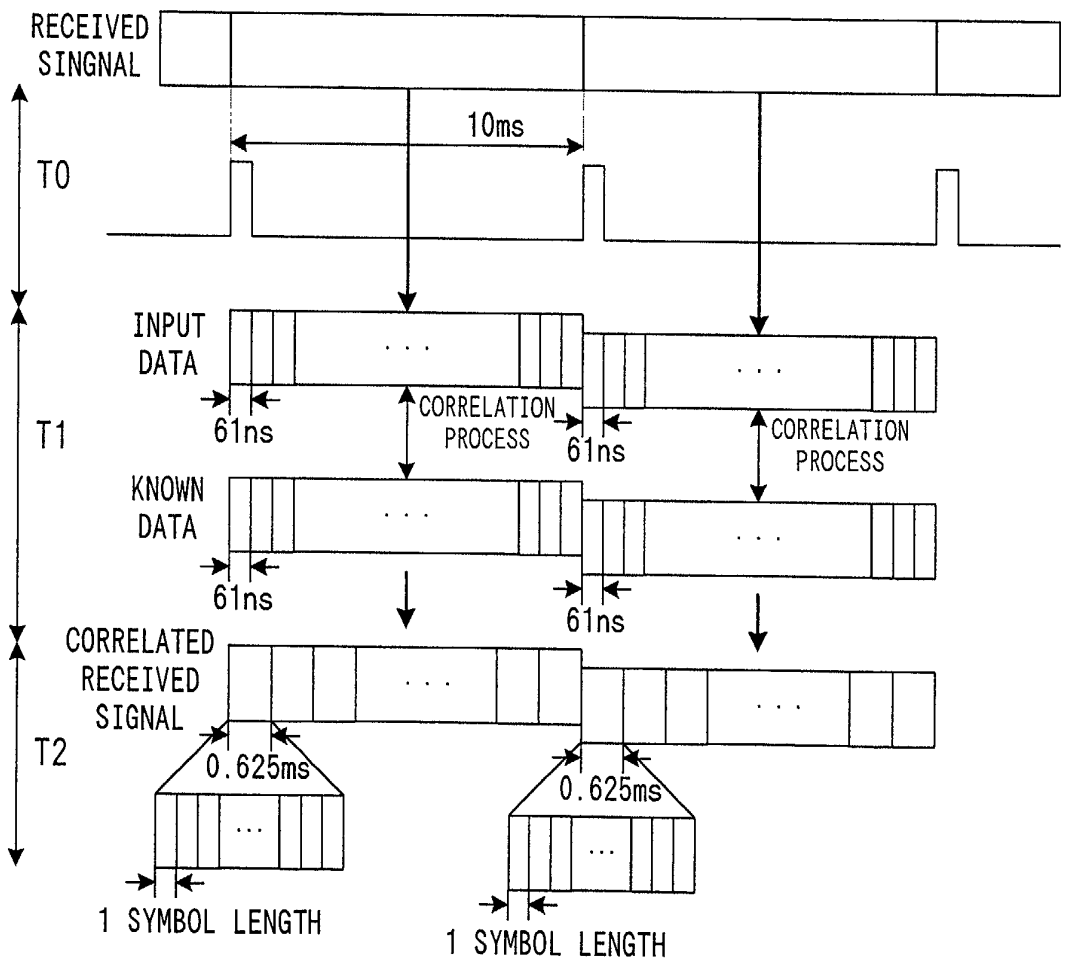

RECEIVED SINGNAL
10ms
T0
INPUT DATA
61ns
CORRELATION PROCESS
61ns
CORRELATION PROCESS
T1
KNOWN DATA
61ns
61ns
CORRELATED RECEIVED SIGNAL
T2
0.625ms
0.625ms
1 SYMBOL LENGTH
1 SYMBOL LENGTH

FIG.5A

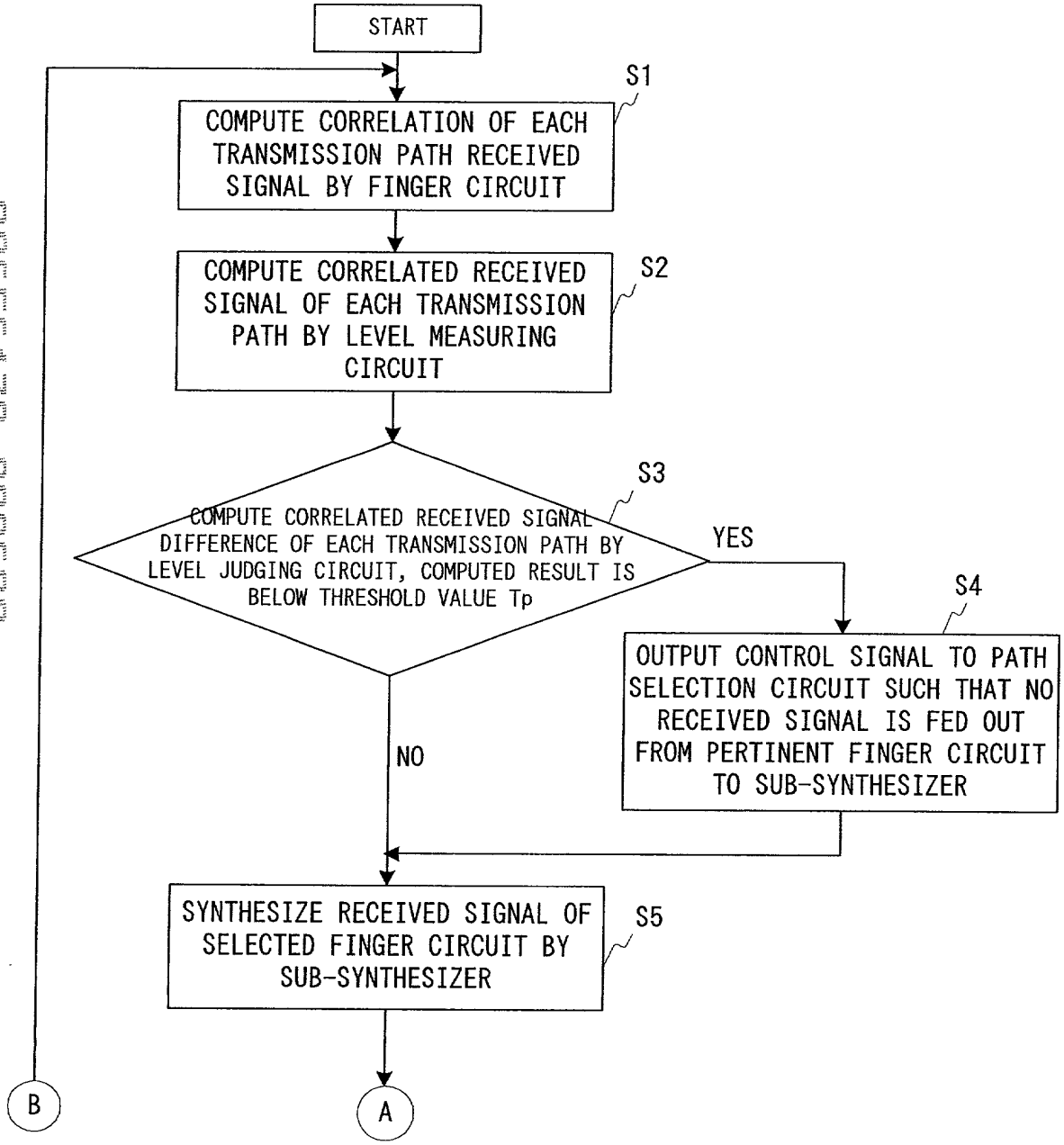

START
S1
COMPUTE CORRELATION OF EACH TRANSMISSION PATH RECEIVED SIGNAL BY FINGER CIRCUIT
S2
COMPUTE CORRELATED RECEIVED SIGNAL OF EACH TRANSMISSION PATH BY LEVEL MEASURING CIRCUIT
S3
COMPUTE CORRELATED RECEIVED SIGNAL DIFFERENCE OF EACH TRANSMISSION PATH BY LEVEL JUDGING CIRCUIT, COMPUTED RESULT IS BELOW THRESHOLD VALUE Tp
YES
S4
OUTPUT CONTROL SIGNAL TO PATH SELECTION CIRCUIT SUCH THAT NO RECEIVED SIGNAL IS FED OUT FROM PERTINENT FINGER CIRCUIT TO SUB-SYNTHESIZER
NO
SYNTHESIZE RECEIVED SIGNAL OF SELECTED FINGER CIRCUIT BY SUB-SYNTHESIZER
S5
B
A

FIG.5B

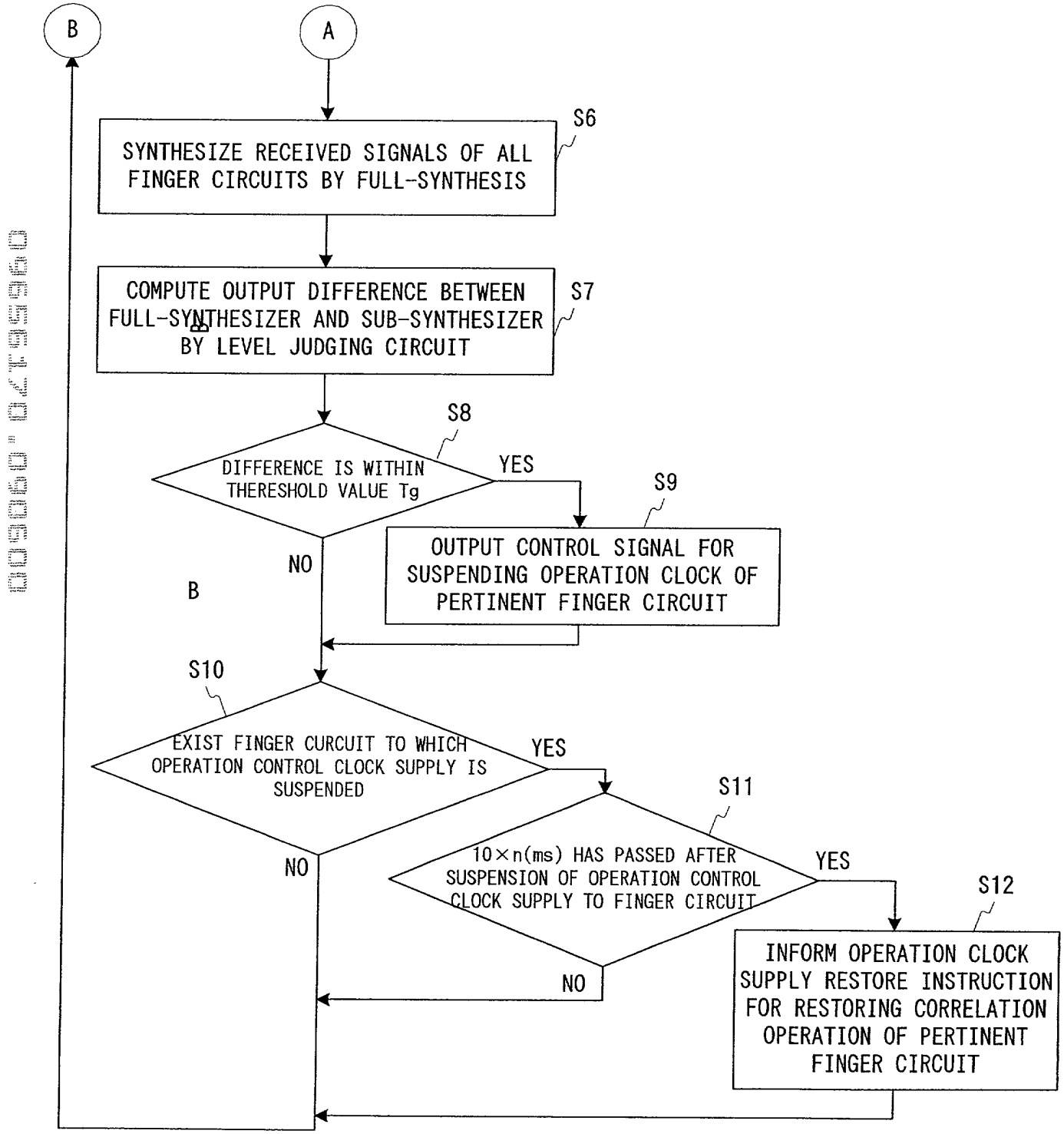

B
A
S6
SYNTHESIZE RECEIVED SIGNALS OF ALL FINGER CIRCUITS BY FULL-SYNTHESIS
COMPUTE OUTPUT DIFFERENCE BETWEEN FULL-SYNTHESIZER AND SUB-SYNTHESIZER BY LEVEL JUDGING CIRCUIT
S7
S8
DIFFERENCE IS WITHIN THERESHOLD VALUE Tg
YES
S9
OUTPUT CONTROL SIGNAL FOR SUSPENDING OPERATION CLOCK OF PERTINENT FINGER CIRCUIT
NO
B
S10
EXIST FINGER CURCUIT TO WHICH OPERATION CONTROL CLOCK SUPPLY IS SUSPENDED
YES
S11
10×n(ms) HAS PASSED AFTER SUSPENSION OF OPERATION CONTROL CLOCK SUPPLY TO FINGER CIRCUIT
YES
S12
INFORM OPERATION CLOCK SUPPLY RESTORE INSTRUCTION FOR RESTORING CORRELATION OPERATION OF PERTINENT FINGER CIRCUIT
NO
NO

FIG.6

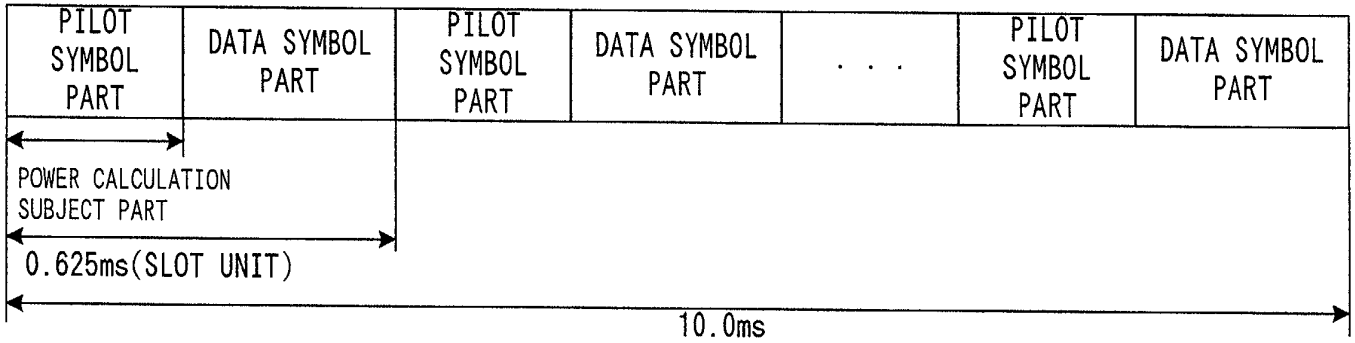

PILOT SYMBOL PART
DATA SYMBOL PART
PILOT SYMBOL PART
DATA SYMBOL PART
. . .
PILOT SYMBOL PART
DATA SYMBOL PART
POWER CALCULATION SUBJECT PART
0.625ms(SLOT UNIT)
10.0ms

FIG.7

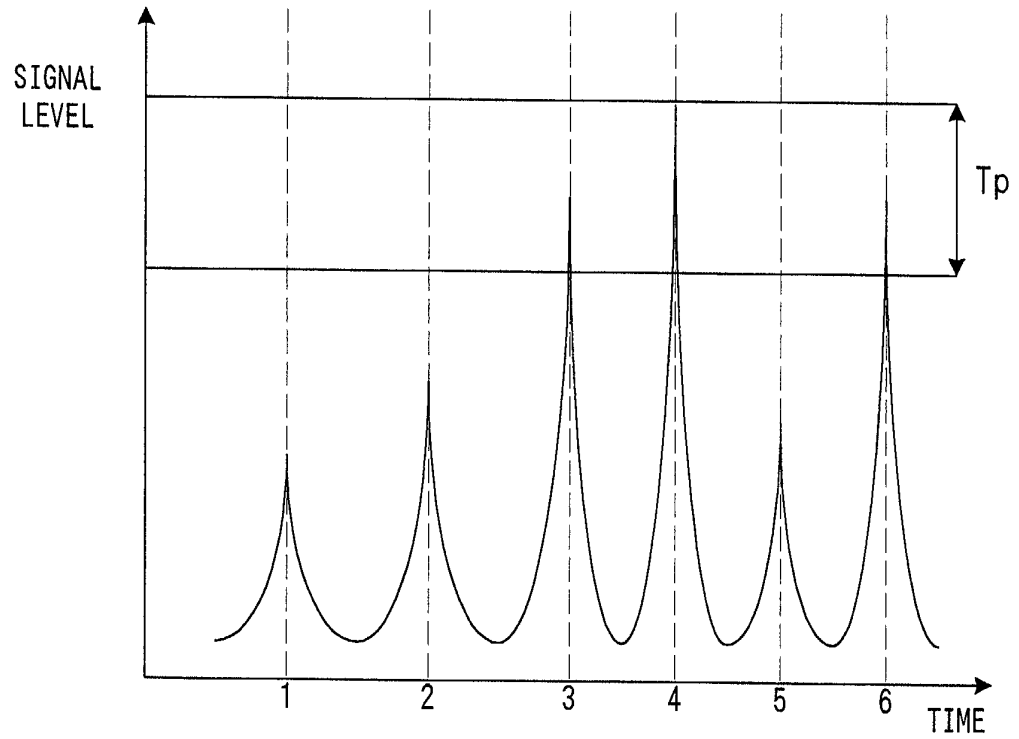
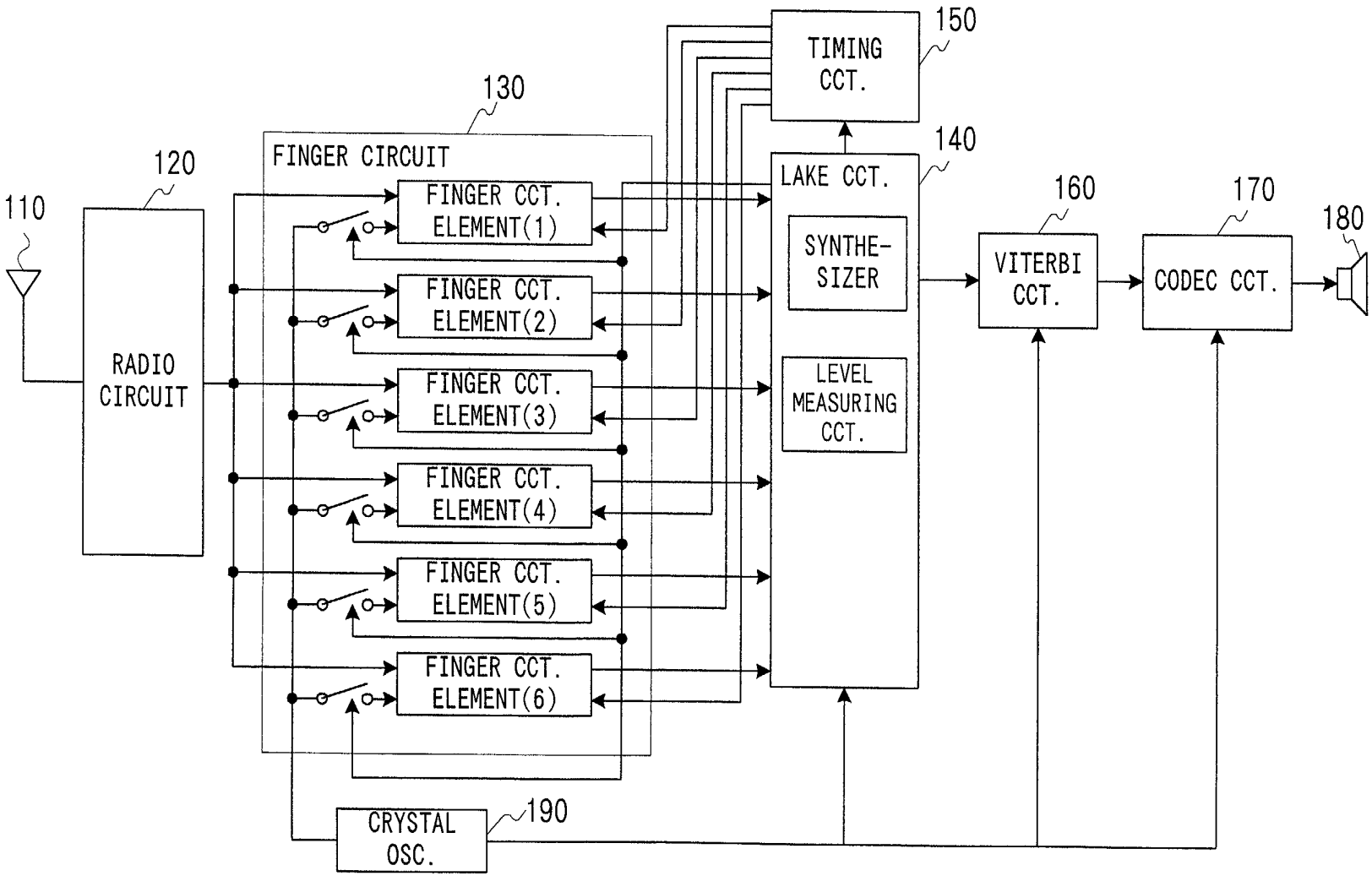


FIG.8


110
120
RADIO CIRCUIT
130
FINGER CIRCUIT
FINGER CCT. ELEMENT(1)
FINGER CCT. ELEMENT(2)
FINGER CCT. ELEMENT(3)
FINGER CCT. ELEMENT(4)
FINGER CCT. ELEMENT(5)
FINGER CCT. ELEMENT(6)
150
TIMING CCT.
140
LAKE CCT.
SYNTHE-SIZER
LEVEL MEASURING CCT.
160
VITERBI CCT.
170
CODEC CCT.
180
CRYSTAL OSC.
190

Docket No _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

RECEIVING TERMINAL, RECEIVER AND RECEIVING METHOD FOR CDMA SYSTEM

the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

NUMBER	COUNTRY	DAY/MONTH/YEAR FILED	PRIORITY CLAIMED
251229/1999	Japan	06/09/1999	Yes

☐ I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

APPLICATION NO.	FILING DATE

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

I hereby appoint as my attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. Stephen A. Bent, Reg. No. 29,768; David A. Blumenthal, Reg. No. 26,257; John J. Feldhaus, Reg. No. 28,822; Donald D. Jeffery, Reg. No. 19,980; Eugene M. Lee, Reg. No. 32,039; Peter G. Mack, Reg. No. 26,001; Brian J. McNamara, Reg. No. 32,789; Sybil Meloy, Reg. No. 22,749; George E. Quillin, Reg. No. 32,792; Colin G. Sandercock, Reg. No. 31,298; Bernhard D. Saxe, Reg. No. 28,665; Charles F. Schill, Reg. No. 27,590; Richard L. Schwaab, Reg. No. 25,479; Arthur Schwartz, Reg. No. 22,115; Harold C. Wegner, Reg. No. 25,258.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address		

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Residence Address		Country of Citizenship
Post Office Address		